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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,509	07/23/2003	Isao Takayanagi	M4065.0905/P905	7407

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EXAMINER
TRAN, NHAN T

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2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/624,509	TAKAYANAGI, ISAO	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) *5,12-50,56 and 61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-11,51-55 and 57-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of **Species I, Fig. 4, claims 1-4, 6-11, 51-55 and 57-60** in the reply filed on 3/9/2007 is acknowledged. The traversal is on the ground that there would not be a serious burden on the Examiner. This is not found persuasive because each of Species I to Species IV is distinct from each other as stated in the previous Office Action. Specifically, Species I does not require averaging multiple frames 500 as required by species II; species III does not require memory array 1009 as required by species IV while species III requires TG1 and TG2 (in each pixel) that are not required by species IV.

Because there are four distinct Species being claimed, there would be separate search required for each species. Thus, there would be a burden on the Examiner.

The requirement is still deemed proper and is therefore made FINAL.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/4/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 51 is rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (US 6,037,577).

Regarding claim 51, Tanaka discloses a memory circuit (charge adding circuit 30 shown in Fig. 7 and details in Fig. 14) comprising:

an input lead (input line 10 shown in Figs. 7 & 14) for receiving a readout signal from a pixel circuit (col. 9, lines 3-24);

a first capacitive clement (32a in Fig. 14) connected to the input lead, the first capacitive element storing a voltage indicating a level of a received readout signal; a second capacitive element (32b); a switching element (49b) connected between the first and second capacitive elements and, when switched on, providing a conductive path through which a previous voltage stored by the second capacitive clement is combined with the stored voltage from the first capacitive element (see Fig. 14 and col. 11, lines 40-60, wherein when the switch 49b is turned on in addition to turning on switch 49a, the signal charge stored in capacitor 32b is combined with the signal charge in capacitor 32a); and a readout element (readout line) connected to provide a readout signal from the first capacitive element when the switching element (49b) is switched off (note that

under normal lighting condition, no charge addition is needed, and therefore only switch 49a is used while switch 49b is off; see col. 11, lines 24-30) and from the first and second capacitive elements when the switching element (49b) is switched on (this is when charge addition is needed and selected according to the low-light condition, where both charges in capacitors 32a and 32b are added by turning on the switch 49b in addition to switch 49a as disclosed in col. 11, lines 24-30 and 40-60).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 52, 55, 57, 60 are rejected under 35 U.S.C. 102(e) as being anticipated by Afghahi (US 6,747,695).

Regarding claim 1, Afghahi discloses an imaging device (Fig. 1 and abstract), comprising:

a pixel array circuit (105) that outputs an image signal and a background signal (i.e., dark signal); a memory array circuit (an array of capacitors in CDS circuit, each CDS 135 contains at least one capacitor 410 shown in Fig. 4), coupled to said pixel

array circuit, said memory array circuit configurable to store an output from said pixel array (see col. 5, lines 1-33); and a data subtraction circuit (CDS 135/DDS 145), coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation on the pixel array output to remove said background signal from said image signal (see col. 5, line 1 – col. 6, line 10).

Regarding claim 4, Afghahi discloses that each memory element in said memory array circuit corresponds to a pixel circuit in said pixel array circuit (Figs. 1 & 4; col. 5, lines 1-33).

Regarding claim 52, this claim is also met by the analysis of claim 1, wherein "a processing circuit" is the whole circuit shown in Fig. 1 of Afghahi.

Regarding claim 55, this claim is also met by the analysis of claim 4.

Regarding claim 57, this claim is also met by the analysis of claim 1, wherein "a substrate" is the semiconductor substrate of the CMOS imager.

Regarding claim 60, this claim is also met by the analysis of claim 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 6-11, 53, 54, 58 & 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Afghahi (US 6,747,695) in view of Goren et al. (US 5,734,152).

Regarding claim 2, Afghahi does not teach an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.

However, as taught by Goren, an edge enhancement filter (30 in Fig. 2a) is provided in an analog domain after a differentiator circuit (4) but before a digital circuit (20) so that the edges of captured image signal are much more pronounced and it is much easier to digitize and decode such an enhanced signal (see col. 6, lines 54-57 and col. 8, lines 15-18).

Therefore, it would have been obvious to one of ordinary skill in the art to implement an analog edge enhancement circuit after the CDS and DDS circuit but before ADC circuit in Afghahi so that the edges of captured image signal are much more pronounced and it is much easier to digitize and decode such an enhanced signal as taught by Goren.

Regarding claim 3, Afghahi in view of Goren also discloses that the imaging device comprises an analog-to-digital converter (ADC 155 shown in Fig. 1 of Afghahi, please also note the analysis of claim 1).

Regarding claim 6, this method claim is also met by the analyses of claims 1 & 2 above. Note that the imager chip is the integrated CMOS imager shown in Fig. 1 of Afghahi and col. 3, lines 28-34.

Regarding claim 7, it is clear in Afghahi that the analog image data is received from a pixel array in said imager chip (see Afghahi, Fig. 1 and col. 3, lines 28-34).

Regarding claim 8, as discussed in claims 1 and 7, the analog image signal is stored in the array of capacitors in the CDS circuit 135 in the imager chip.

Regarding claim 9, Afghahi discloses that the background signal comprises an offset variation signal (i.e., dark current offset variation) (see claim 1).

Regarding claim 10, it is also seen in Afghahi that the dark current noise also imposes fixed pattern noise by inherency (col. 1, lines 44-55).

Regarding claim 11, as discussed in claim 2 above, the combined teaching of Afghahi and Goren teaches that the step of performing an analog-to-digital conversion to the edge-enhanced signal is in said imager chip (integrated imager of Afghahi).

Regarding claims 53 & 54, these claims are also met by the analyses of claims 2 & 3, respectively.

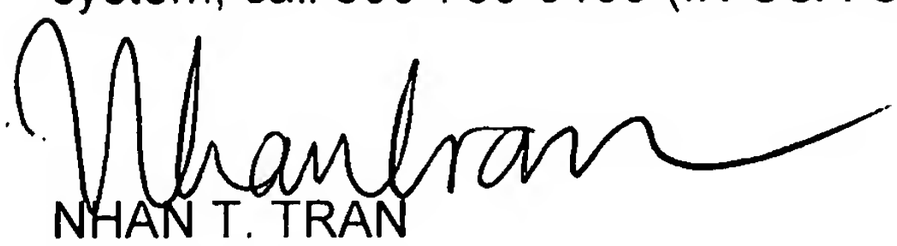
Regarding claims 58 & 59, these claims are also met by the analyses of claims 2 & 3, respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



NHAN T. TRAN
Patent Examiner